FERMI—A New Generation of Electronic Modules for Large Data Acquisition Arrays Required by High Energy Physics

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Abstract— **The FERMI, Front End Readout MIcrosystem, is representative for a new generation of data acquisition modules which utilizes modern design techniques to achieve high acquisition rates together with intelligent on-line data processing. FERMI is being designed to satisfy the extreme requirements set by calorimeters in the next generation of particle physics detectors. Such detectors are currently being designed for the future LHC accelerator at CERN in Switzerland. The calorimeters demand frequent (40 MHz or 80 MHz, if sampled between bunch crossings) high precision sampling of a large number of input channels (about 5.10^5).**

Each FERMI module serves 9 channels from which samples are AD-converted, corrected and temporarily stored in a local memory. The data is also merged into a trigger sum, which is processed by digital filters to determine the arrival time and amplitude of incoming pulses. Such data is then fed to a first-level trigger processor which screens irrelevant information. Only data that may contain useful information is kept for further analysis.

Arrays of 50000 FERMIs constitute a formidable processing system when considering its total computational power and storage capacity.

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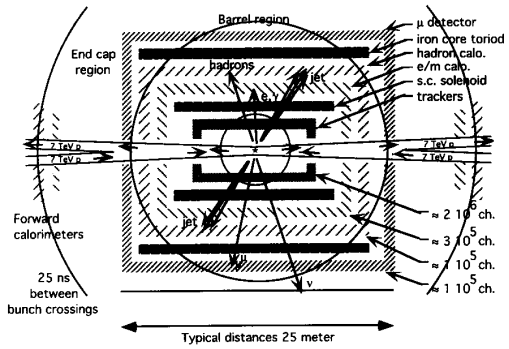


Fig. 1. A typical LHC detector.

I. Introduction

THE NEW PHYSICS content in the data produced by detectors at the next generation of high energy proton accelerators is deeply buried in large amounts of background information. Only one in about 10^9 recorded events contain useful information about unanswered questions in physics. It is therefore crucial that the particle fluxes are sufficiently large to compensate the low yield.

One such accelerator is presently being designed at CERN, in Switzerland, the Large Hadron Collider (LHC). In its 27 km circumference accelerator rings, counter rotating proton beams intersect in collision regions around which detectors are built to record the debris from the proton collisions. Here, protons will be accelerated in several steps until they reach energies of 7 TeV (tera-electron volts). The protons travel in well defined bunches that collide every 25 ns. Each bunch crossing will cause about 40 inelastic proton collisions in each of the different collision regions of LHC.

The detectors are built in layers with different subdetectors sensitive to different aspects of the reaction products. The volume immediately surrounding the collision region contain tracking detectors which record ionization paths from charged particles. These subdetectors may contain as much as 10^7 channels, which fortunately are rather sparsely activated. Furthermore, if the tracking subdetectors are situated in a magnetic

field it will be possible to estimate momentum and charges from the curvature of the particle trajectories.

Outside the trackers there are energy detectors, or calorimeters, of two types, designed to absorb particles. The first and innermost type absorbs electrons and photons, while the second absorbs hadrons. Muons are detected in the outermost subdetector. The presence of non-interacting particles, like neutrinos, can be deduced by summing the momenta of all reaction products from a collision. If all particles are accounted for, the total momentum should vanish.

Recording all information is presently not possible and in any case not meaningful, even if it was. The total amount of data is in the order of hundreds of TBytes/s The strategy chosen is to filter events in steps, trigger levels, until sufficient data reduction is achieved. The first-level trigger makes a rough calculation based on low resolution data from a subset of the detector. This information is sufficient to reject most data, attaining a reduction rate of about 10^3 or 10^4. Data accepted by the first-level trigger is then sent to the second-level trigger, which uses high resolution data within a few limited but relevant regions-of-interest chosen according to information supplied by the first-level trigger. The second-level trigger uses data from all sub-detectors as a base for a decision. A further reduction of about 10^2 may be obtained in this way. In the final trigger step, the third-level trigger, all data is considered, at full resolution, to get a final reduction of about 10^2. The total data reduction achieved in this way is thus in the order of 10^7–10^8. The quality of the trigger algorithms are, however, crucial to the success of the entire experiment. They must be as unbiased, efficient and selective as possible.

The values for the trigger processing times (latencies) are currently estimated to about 2 μs and 2 ms for the first and second-level triggers respectively. This means that all data must be stored in temporary memories during $\sim$2 μs waiting for the first-level trigger decision. The 1% that was not rejected by the first-level-trigger must be kept for $\sim$2 ms.

II. The FERMI Data Acquisition Module

The FERMI data acquisition module is designed to sample, digitize and temporarily store calorimeter data every 25 (or possibly 12.5) ns, while providing reduced precision data for the first-level trigger. The storage should thus be sufficiently large to keep all data for $\sim$2 ms and some data, i.e. the data approved by the first-level trigger, during $\sim$2 μs. Data approved by the second-level trigger as well is kept in storage until it can be read out to the third-level trigger.

FERMI is implemented as a silicon-on-silicon multichip microsystem [1], [2], [3], where the microsystem is a chip carrier with a large silicon multi-layer substrate serving as an active circuit board on which integrated circuits are bonded. The substrate also contains diffused and surface-mounted components, interconnections and transmission lines.

A FERMI prototype module is being developed within a research and development program at CERN, RD-16, approved by the CERN Detector Research and Development Committe (DRDC) in April 1991. The FERMI collaboration, now consisting of nine research institutes and three industrial partners, was thus formed with the aim to explore and develop the technologies required to implement the FERMI prototype.

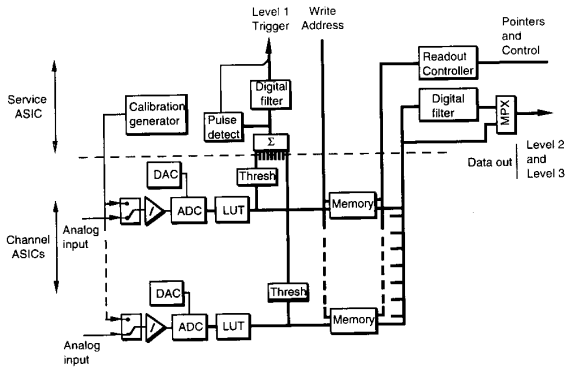


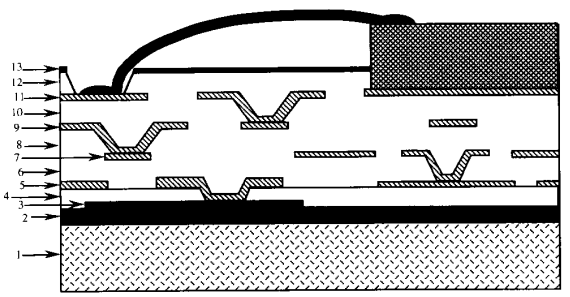
Fig. 2. An overview of the FERMI data acquisition module.

Fig. 2 contains all major FERMI components in the form of a simplified block diagram. It is divided into two main parts: an acquisition part and a common service part. The former consists of nine identical channels, while the latter is unique. To achieve sufficient reliability, FERMI is being designed with a high degree of fault tolerance and will partially be implemented in rad-hard process technologies. These qualities are important since FERMI will probably be mounted on the calorimeter surface well inside the detector, where the ambient radiation level is fairly high.

The precision and dynamic range of FERMI should match that of the calorimeter used, so that it does not significantly compromise the data. It has been found that this can be achieved with a 10-bit AD-converter, provided a suitable analog compression has been applied prior to the conversion. This is done in a non-linear amplifier stage. After conversion, data is expanded to a linear 16-bit representation by applying the inverted non-linearity via a look-up table. This device can also incorporate an absolute calibration for each individual channel.

Sufficiently large channel values, i.e. values well above the assumed noise level, are summed and processed in order to provide energy and bunch crossing time information to the first-level trigger processor. A module-level pulse detect signal can warn for possible pile-up conditions so that the corresponding channel can be subjected to special processing. This occurs when two successive pulses appear close enough in time to disturb each other's pulse shapes.

The expanded data are also stored in a dual-port memory, waiting for decisions from the first and second-level triggers. The memory locations are supplied by an external memory management unit, the address generator [4], which extracts pointers from a pool of free memory pointers. A temporal environment, a time frame of programmable length, is associated with each event accepted by the first-level trigger. After the first-level decision, all memory locations containing sample points not included in a time frame are returned to the pool of free memory. Time frame memory locations are also returned



1	Si	8	BCB2
2	SiO2	9	Al (metal 3)
3	TiN	10	BCB3
4	SiOxNy	11	Al (metal 4)
5	Al (metal 1)	12	BCB4 (passivation
6	BCB1	13	SiO2 (BCB protection)
7	Al (metal 2)		

Fig. 3. Cross section of the microsystem substrate process.

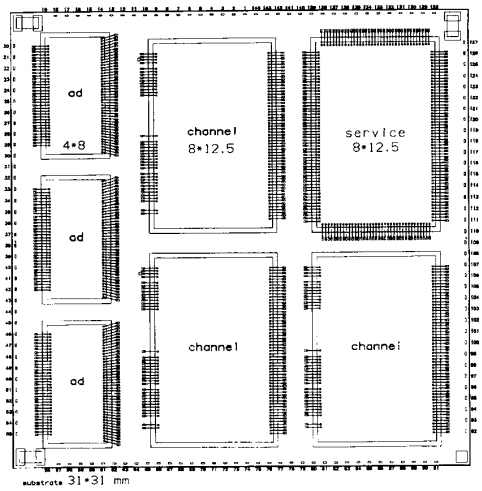


Fig. 4. Floorplan of the FERMI microsystem.

to the free pool after having been rejected by the second-level trigger or after the final read out to the third-level.

The FERMI I/O facility contains provisions for full or reduced readout of time frames. In the latter case the information contained in the time frame is extracted by means of adaptive non-linear digital filtering techniques. It is envisaged that the reduced readout should be default when pushing data to the second-level trigger processors. These could, however, also return for selective readout of full time frames, an option which might be used in order to resolve specific conditions.

III. Microsystem

The FERMI microsystem is implemented as a thin-film Multi-Chip Module (MCM-D). This means that several ASIC dies are mounted on top of a thin-film substrate containing interconnections, integral resistors and capacitors. The actual process used for FERMI is based on a silicon substrate. Four metal layers are used, two for interconnections and two for power distribution. The dielectric between the metal layers is Benzocyclobutene (BCB) with a low dielectric constant. The resistors are realised in a TiN-layer and the capacitors are formed between the TiN-layer and first metal with siliconoxynitride as dielectric. A cross section of the process is shown in Fig. 3.

Some of the main characteristics of the process are given below:

- Signal line width, 25 μm
- Spacing between lines, 50 μm
- Characteristic impedance, $Z_0 = 50 \pm 5\ \Omega$

Transmission calculations [8] show that the output driving current of an IC can be reduced by a factor of 5 in a design like FERMI using microsystem technology instead of a conventional PCB solution. This reduction of output drive current will contribute directly to a reduction of power supply noise by the same factor. In order to decrease the power supply noise further, the influence of die to substrate interconnect was investigated. Using flip-chip bonding between the ICs and the silicon substrate power supply noise can be reduced further to 1/20 of that with conventional wire-bonding in the FERMI microsystem. Based on this it was decided to evaluate the possibilities to mount the ICs in the FERMI microsystem by flip-chip assembly on the substrate.

For the FERMI system a number of package options will be available. Results from irradiation tests show that for the final solution a plastic package is preferable, since it contains only small amounts of substances that are susceptible to neutron activation. For the prototypes existing ceramic packages (ceramic PGA, 50 × 50 mm cavity, 200 I/O) will be used, with the advantage of easier testing and design evaluation. These packages would, however, not be optimized for crosstalk or with respect to radiation effects. The final choice will be based on the results of the evaluations of prototypes as well as the mechanical design of the complete data acquisition system.

Fig. 4 shows the preliminary version of the FERMI microsystem floorplan. The floorplan design is based on the following preliminary die sizes: channel IC = 100 mm^2, service IC = 100 mm^2 and A/D IC = 32 mm^2. The analog switches and dynamic range compressors are implemented on the A/D-analog chips. To reduce crosstalk from the digital right side to the analog left side, the power and ground planes are split over the AD-chips into an analog left side and a digital right side. The microsystem has approximately 100 I/O connections, which leaves 100 pins for power supply and test signals in the prototype package.

From the characteristics of the process given above, the maximum crosstalk between two signal lines on the substrate is −34 dB. This is the value between two parallel lines at the closest pitch of 75 μm as measured at the first resonance frequency. In FERMI the crosstalk is minimised by using solid power and ground planes, by placing guard strips between signal lines and allowing for 2.5 mm between lines carrying the input signals. This approach will therefore provide conditions similar to those in a coaxial cable for the analogue transmission lines in the module.

IV. Fault Tolerance

FERMI will be placed in a position where full experimental information concerning fault mechanisms is not yet available. The lack of accurate information on such characteristics as fault distribution in space and time, the dependence of fault rate on accumulated dose, the correlation between faults and the exact nature of these faults prevents the development of a complete fault model of the system. As a consequence, the strategy adopted for providing some degree of fault tolerance has to be quite general. It must take into account survival when exposed to single or multiple faults and a suitable balance between graceful degradation and full error correction.

A fundamental point that has to be accounted for concerns the balance between area overhead and actual reliability of the final device. In the specific case of FERMI the most suitable solution for fault tolerance seems to be a combination of techniques dealing with error detection, error correction and dynamic redundancy. It was therefore decided to provide:

- single or multiple fault detection within individual subsystems of each acquisition channel, by means of error correction codes (ECC) (linear, e.g. extended Hamming, or modulo-3, for busses and arithmetic units, respectively)
- immunity to single faults within individual subsystems of each acquisition channel by means of ECC or hardware redundancy.
- diagnostic information via host-driven actions

Fault tolerance is thus implemented in FERMI in different ways, depending on the logical function of each stage. It can be automatic as in memories with error correction codes (ECC), or it may require controller intervention. In the latter case online or ordered error checking will alarm the module controller, which will respond with a possible hardware reconfiguration. In functions with a high level of parallelism, it is usually straightforward to add spare parts. Another method is to use voting procedures on parallel data paths. One way to accomplish this is to triplicate sensitive functions that has not been protected in other ways, merging the outputs into one node. With CMOS technology the majority level will rule the merger node, be it high or low. This current voting procedure has the advantage that it does not add fault sensitive overhead such as voting circuitry. An additional safety factor is a small associative memory operating in parallel with the main data memory used for patching faulty cells. It can also be used for diagnostic purposes.

In the analog part, radiation damage will introduce a smooth degradation of performance. The reliability of this part is provided by the programmability of the look-up table and the calibration and linearization functions built into the FERMI architecture. This also includes the analog part of the A/D converter.

Error detection must be capable of identifying the presence of at least one error within the considered function. Single-bit errors should be corrected, while double-bit error detection is adopted to identify invalid data. In addition, the availability of some degree of redundancy will increase system survival in case of independent multiple faults and/or permanent faults. The approaches adopted for the various digital subsystems are briefly described in the "Digital part" section below.

In order to investigate the fault mechanisms inherent to the FERMI design during its normal operating conditions, efforts have been made to estimate the effects of the radiation doses and types encountered in its operating environment. The expected dose of electromagnetic radiation and neutron flux inside the future LHC detectors have been calculated using an updated version of the FLUKA program [5]. The electromagnetic radiation will mostly cause single event upsets, while the neutron radiation will cause errors to occur in many places at about the same time. This is due to the fact that defects from a large number of neutrons are required to cause an error. The neutron radiation can also affect the operation of the device by activating surrounding material which then will serve as a secondary source of electromagnetic radiation.

V. The FERMI System Environment

FERMI relies on external circuitry to provide control sequences and to read out data. If a number of FERMIs are mounted on a board, this circuitry can be of considerable complexity. It will probably have to provide the following functions:

- Local first-level trigger: to combine data from several FERMIs into one trigger-cell value, which is transmitted to the global first-level calorimeter trigger.
- Local second-level trigger: to read data from several FERMIs and to transmit them to the second-level trigger processor.
- Memory management: to generate new addresses each 25 (or 12.5) ns, pointing at free storage locations for the sampled input data and to generate the pointers required for readout.
- Controller : to initialize, control and supervizethe FERMIs.

These functions must be extremely fault tolerant, since any failure will seriously reduce the functionality of the entire system. Such a fault tolerance is very difficult to achieve with standard random logic. Different (partial) solutions can be envisaged;

- Moving as much as possible of the functionality out of the detector will relax the fault tolerance requirement. A good fault detection strategy will identify and localize faults, so that the erroneous part may be replaced.
- Moving functions into FERMI will also relax the fault tolerance requirement, since the consequences of faults are then only local to a given FERMI. Furthermore, the necessary fault tolerance is also easier to realize in the ASICs of the microsystem.
- Grouping as much as possible of the remaining circuitry into a dedicated ASIC, a FERMI board controller, where fault tolerant multiply redundant circuit solutions can be used.

Another important issue is how to solve the communication problems. Coaxial cables take up space and limit transmission speed. Optical fibers, however, are superior in both respects. The coupling between optical receivers and transmitters and

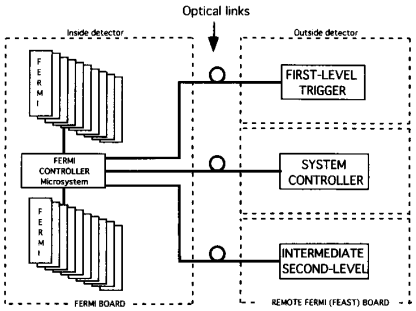


Fig. 5. The FERMI system environment.

the ASICs is easiest realized in a multichip microsystem. A reasonable solution is therefore to collect all the functions that cannot be relocated to the outside of the detector into one fault-tolerant microsystem, a FERMI controller microsystem, which will communicate electrically with the FERMIs and optically with the system controller, first and second-level triggers. One of the relocated functions could be the address generator, which then would be global. This has the advantage of eliminating the loss of synchronism between local address generators as a possible source of errors.

A 1 Gb/s two-way optical link is sufficient for communication with the second-level trigger for a board containing about 36 FERMIs. This connection can also provide a communication channel for control and status reporting. Two similar fibers can transmit addresses from the address generator, the 40 (or 80) MHz bunch crossing clock, as well as test and global command pulses. The communication with the first-level trigger could probably be handled by nine such fibers. Fig. 5 shows a possible implementation of these ideas.

VI. Digital Filters

The filter functions of FERMI consist of two different digital filter sections. The first filter is designed to identify a signal providing accurate timing information and relatively coarse energy information for the first-level trigger. It operates on the sum of the nine FERMI channels, while the single channel data are stored in a data memory. Only data accepted by the first-level trigger will be transferred to the second filter.

The second filter is designed to extract an accurate value for the energy provided the sample timing jitter is the dominant source of error. Time frame data can be extracted by bypassing the second filter under special conditions, e.g. for particular classes of interesting events or when a severe pileup condition is detected. Also, two different coefficient banks are available to tailor the filtering to different conditions on an event-by-event basis.

A. The First-Level Trigger Filters

The first-level trigger filter is composed of the summing unit, which adds individually thresholded data from the nine channels of a FERMI, and two FIR filters operating on the channel sum.

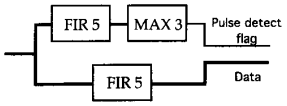


Fig. 6. First filter structure for the prototype.

The optimal strategies for extracting time and energy information may be different, and the hardware for the prototype is designed to provide the maximum flexibility for exploring and optimizing both algorithms separately. This is achieved by using two parallel FIR filter branches (see Fig. 6): the timing is determined using a 5-tap FIR filter optimized for time measurements, followed by a three-point maximum finder. The energy is measured using another 5-tap FIR filter optimized for amplitude measurement.

The filter coefficients for both cases can be obtained using either analytical techniques or a least mean square (LMS) error optimization technique with a training set containing signals of different heights and different noise content.

Three different modular architectures have been examined:

i) a conventional architecture based on multiplier modules,
ii) an architecture based on single-bit convolvers [6]
iii) an architecture with parallel barrel shifters and no multipliers.

The third architecture, has been chosen for the prototype because of its inherent simplicity and high speed. It differs from the two other solutions in the fine-grained quantified representation of the FIR filter coefficients. Using only two barrel shifters (both of which can negate the output value) the coefficient values in the range e.g. $(-3, 3)$ can be covered so uniformly and with sufficient precision that the performance requirements of the first-level filters are met without relying on complex multiplier structures.

The resolution of the timing filter, simulated under pessimistic noise and jitter conditions, is such that at 500 MeV, the error rate is 4.7% for the training method and 1.6% for the analytical method. For energies above a few GeV no errors have been detected. The fraction of events erroneously ascribed to adjacent bunch crossings is less than $5\ 10^{-5}$.

B. The Second-Level Trigger Filter

The task of the second-level trigger filter is to measure the pulse amplitude with very high precision using the time frame identified by the first-level trigger. This filter has to provide full accuracy in the presence of sample timing jitter and different noise components. If a pileup condition is detected, a different set of filter coefficients is used. If the pileup is considered too severe, or for special events, the whole time frame can be read out.

In order to measure the pulse amplitude with very high precision, a non-linear feature extraction method is used. The filter consists of a bank of linear FIR filters, followed by an order statistic operator function. The order statistic operator sorts the input values in ascending order and selects the rth largest of them as the operator output. This non-linear filter structure is best suited for pulse height measurement when

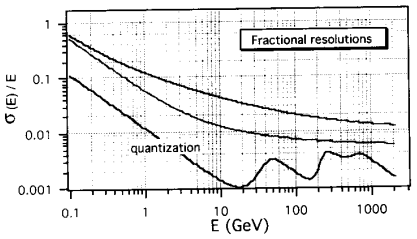


Fig. 7. Measured fractional resolutions of the compressor—ADC system compared to that of two typical calorimetric detectors.

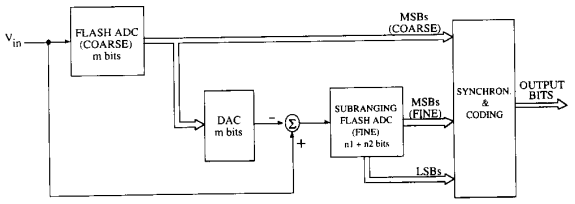


Fig. 8. Block diagram of the two-stage pipelined ADC architecture.

the sampling positions are fluctuating; the FIR subfilters are adapted to different jitter conditions and the order statistic part selects one of them according to the outputs of the FIR filter bank. The procedure to obtain the optimal coefficients for an adaptive FIR/order statistic hybrid (AFOSH) filter is explained in [7]

VII. THEANALOG PARTS

A. Compression

A FERMI module receives analog signals with a dynamic range of about 15–16 bits. To fit these signals inside the range of the 10-bit ADCs require a dynamic range compression at the analog input level. This can be done adding only a negligible contribution to the total detector resolution, provided the non-linear transfer function is matched to the resolution of the calorimeter [1].

A piecewise linear transfer function, where the input signal is amplified in stages with different gains and the outputs added linearly, has been chosen. Two different solutions, a bipolar and a CMOS version, have been developed.

Fig. 7 shows the measured fractional resolution of a prototype of the bipolar compressor, compared with the fractional resolutions of two typical detectors. The contribution of the quantization noise to the total resolution is minimal, even for a high quality calorimeter.

B. Sampling and A/D Conversion

Two different approaches to the analog to digital conversion are being followed, a Two-Stage Pipelined A/D converter and an array of Successive Approximation converters (PSA-ADC). A final choice will be made once prototypes of both types will have been thoroughly tested.

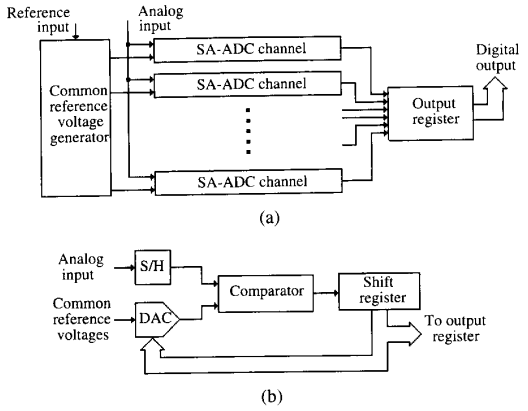


Fig. 9. Block diagram of the PSA-ADC. (a) A PSA-ADC. (b) An SA-ADC.

The Two-Stage Pipelined A/D Converter: Fig. 8 shows the topology of the two-stage pipelined A/D converter architecture.

A first coarse conversion is carried out by means of a flash ADC, to obtain the m most significant bits (MSBs). The converted bits are then fed to a D/A conversion stage to generate an analog voltage which is subtracted from the input signal. The residue is then converted by a subranging ADC, which gives the remaining $(n_1 + n_2)$ least significant bits (LSBs). Finally, the $(m + n_1 + n_2)$ bits are synchronized to generate the output digital word. In order to reach an accuracy of 10 bits, and to compensate for errors arising in the subtraction and from mismatches between the coarse ADC and the DAC, the resolution of the coarse flash converter is increased by one bit, i.e. $m = 5, n_1 + n_2 = 6$. The 11 bits are processed by a digital encoder generating the 10-bit output word.

The Parallel Successive Approximation ADC: The principle of the Parallel Successive Approximation ADC (PSA-ADC) is shown in Fig. 9(a).

A full converter includes a number of identical successive-approximation ADC (SA-ADC) channels, a common reference voltage generator and an output register. The number of channels is given by $(k + n)$, where k is the number of clock cycles needed for comparator auto-zeroing and n is the number of bits. Each channel comprises a S/H circuit and a successive approximation ADC. Each SA-ADC, shown in Fig. 9(b), comprises an auto-zeroed comparator, a shift register and a digital-to-analog converter (DAC). The output register collects digitized data from each channel and pipelines them to the output.

The parallel architecture allows high conversion speed by using low speed SA-ADCs. Since each channel is efficient, the cost of such a parallelism is low. Because of its high efficiency, a 10-bit PSA-ADC needs only 14 comparators, in contrast with 62 comparators for a half-flash ADC or 1023 comparators for a full-flash ADC. Therefore, the power consumption is substantially reduced. It consumes one third of the power of a half-flash ADC and much less power than a full-flash ADC. A PSA-ADC prototype has been tested and found to achieve full 10-bit resolution up to 70 MHz.

VIII. Design Methodology

The entire digital part of FERMI is defined using VHDL (VHSIC Hardware Description Language). The connectivity of the system is described using schematics. These schematics can be converted to structural descriptions to obtain a VHDL description of the whole module. In order to allow the use of different design tools appropriate modifications have to be introduced in the code. They have been added in such a way that different versions of the code, e.g. for simulation and for synthesis, can be generated from the basic source models using a macro preprocessor. The ASIC implementations are verified using test vectors generated from the VHDL simulations.

Before transferring the VHDL code into the first silicon ASIC prototype, a final verification using FPGAs (field programmable gate arrays), will be done. This approach allows you to:

- record real signals and compare them with simulated ones.
- provide hardware for the test bench to test software routines before the demonstrator is completed.
- optimize and iterate the description of the digital part before final implementation.

The breadboard prototype is implemented on VME boards integrated into the FERMI test bench. Its output is fed to a fast dual-port memory and read out with LABVIEW software. A VME interface allows to load and monitor the hardwired synthesized VHDL FERMI code.

IX. Conclusion

The design of the FERMI module is well under way. The aim is to fabricate a prototype module in the spring of 94. Large parts of the analog parts have already been produced and tested. After the first round of tests the FERMI prototype will most certainly proliferate into a family of modules adapted for different environments.

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